AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A bi-directional shift controller ~~device operable to receive an input from either of two shift registers and provide an input to a shift register input,~~ comprising:

a first control line with a first voltage;

a second control line with a second voltage;

a plurality of ~~devices~~ transistors serially connected between a first control line and a third voltage ~~known voltage~~, wherein ~~a first terminal of a first one of said devices~~ the second terminal of the first transistor is electrically connected to said first control line and ~~a second~~ the drain terminal of said first ~~device~~ transistor is electrically connected to ~~a first terminal of a second one of said devices and a second terminal of a third one of said devices is connected to said known voltage;~~ the second transistor, and the source terminal of the third transistor is connected to said third voltage;

a fourth ~~device~~ transistor connected between a second control line and ~~said shift register input~~ an input terminal of a shift register stage, ~~said first device second terminal~~ the drain terminal of said first transistor further electrically connected to said ~~shift register~~ input terminal of said shift register stage;

means to apply a first output voltage from previous shift register stage

concurrently to ~~a third terminal~~ gate terminals of each of said first ~~and one of said second and third devices~~ and third transistors; and

means to apply a second output voltage from next shift register stage concurrently to gate terminals of each of said fourth transistor.

~~means to apply a second voltage concurrently to a third terminal of each of said fourth and the other one of said second and third devices; and~~

~~means to apply different voltages to said first and second control lines, wherein said different voltages determines which of said adjacent shift register inputs is processed.~~

2. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 1, further comprising:

means to invert said first and second voltages.

3. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 1, wherein said first, second, third, and fourth transistors provide a combinatorial logic ~~is~~ operable as a NOR gate.

4. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 3, wherein said first and fourth ~~devices~~ transistors are n-type ~~devices~~ and said second and third ~~devices~~ transistors are p-type ~~devices~~.

5. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 3, wherein said ~~known~~ third voltage is ~~a high voltage~~ V_{dd}.

6. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim ~~3~~ 5, wherein said first control line voltage is ~~a high voltage~~V_{dd} and second control line voltage is ~~a low voltage~~ V_{ss}, wherein V_{dd} is higher than V_{ss}.

7. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim ~~3~~ 5, wherein said first control line voltage is ~~a low voltage~~V_{ss} and second control line voltage is ~~a high voltage~~ V_{dd}, wherein V_{dd} is higher than V_{ss}.

8. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim ~~2~~ 1, wherein said first, second, third, and fourth transistors provide a combinatorial logic ~~is~~ operable as a NAND gate.

9. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 8, wherein said first and fourth ~~devices~~ transistors are p-type ~~transistors~~ and said second and third ~~devices~~ transistors are n-type ~~transistors~~.

10. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 8, wherein said ~~known~~ third voltage is ~~a low voltage~~ V_{ss}.

11. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim ~~8~~ 10, wherein said first control line voltage is ~~a high voltage~~ V_{dd} and second control line voltage is ~~a low voltage~~ V_{ss}.

12. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim ~~8~~ 10, wherein said first control line voltage is ~~a low voltage~~ V_{ss} and second control line voltage is ~~a high voltage~~ V_{dd}.

13. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 1, wherein said ~~devices~~ transistors are selected from the group consisting of~~:~~ ~~FET, FGT,~~ field effect transistors and floating gate transistors.

14. (Currently Amended) The ~~device~~ bi-directional shift controller as recited in claim 1, wherein said shift ~~registers~~ register stages are physically adjacent to said ~~device~~ bi-directional controller.

15. (Currently Amended) The ~~device~~ bi-directional shift controller circuit as recited in claim 1, wherein said shift ~~registers~~ register stages are logically adjacent to said ~~device~~ bi-directional controller.

16. (Currently Amended) A bi-directional shift register circuit comprising:

a first control line with a first voltage;

a second control line with a second voltage;

a plurality of shift ~~registers~~ register stages, each of the shift register stages having an input terminal and an output terminal, and

a bi-directional shift controller ~~circuit associated with each of said shift registers~~ comprising:

~~a first input connected to a first shift register output terminal and a second input connected to a second shift register output terminal;~~

a plurality of transistors serially connected between a first control line and a third voltage, wherein the source terminal of the first transistor is electrically connected to said first control line, and the drain terminal of said first transistor is electrically connected to the second transistor, and the source terminal of the third transistor is connected to said third voltage;

the fourth transistor connected between a second control line and an input terminal of a shift register stage, the drain terminal of said first transistor further electrically connected to said input terminal of said shift register stage;

means to apply a first output voltage from previous shift register stage concurrently to gate terminals of each of said first and third transistors; and

means to apply a second output voltage from next shift register stage concurrently to gate terminals of each of said fourth transistors.

~~means to apply a first and a second control voltage, wherein said first and second control voltage are different; and~~

~~a combinatorial circuit responsive to said first and second control voltages to apply an indication of an input received from either said first shift register or said second shift register to said corresponding shift register input terminal.~~

17. (Canceled)

18. (Currently Amended) The ~~device~~ bi-directional shift register circuit as recited in claim ~~17~~ 16, further comprising:

means to invert voltages on said first and second inputs.

19. (Currently Amended) The ~~device~~ bi-directional shift register circuit as recited in claim ~~17~~ 16 wherein said first, second, third, and fourth transistors provide a combinatorial circuit ~~is selected from the group consisting of:~~ operable as an NOR~~,~~ ~~NAND~~ gate.

20. (New) The bi-directional shift controller as recited in claim 19, wherein said first and fourth transistors are n-type and said second and third transistors are p-type.

21. (New) The bi-directional shift controller circuit as recited in claim 19, wherein said third voltage is V_{dd}.

22. (New) The bi-directional shift controller circuit as recited in claim 21, wherein said first control line voltage is V_{dd} and second control line voltage is V_{ss}, wherein V_{dd} is higher than V_{ss}.

23. (New) The bi-directional shift controller circuit as recited in claim 21, wherein said first control line voltage is V_{ss} and second control line voltage is V_{dd}, wherein V_{dd} is higher than V_{ss}.

24. (New) The bi-directional shift controller circuit as recited in claim 16, wherein said first, second, third, and fourth transistors provide a combinatorial logic operable as a NAND gate.

25. (New) The bi-directional shift controller circuit as recited in claim 24, wherein said first and fourth transistors are p-type and said second and third transistors are n-type.

26. (New) The bi-directional shift controller circuit as recited in claim 24, wherein said third voltage is V_{ss}.

27. (New) The bi-directional shift controller circuit as recited in claim 26, wherein said first control line voltage is V_{dd} and second control line voltage is V_{ss}.

28. (New) The bi-directional shift controller circuit as recited in claim 26, wherein said first control line voltage is V_{ss} and second control line voltage is V_{dd}.

29. (New) The bi-directional shift controller circuit as recited in claim 16, wherein said transistors are selected from the group consisting of field effect transistors and floating gate transistors.

30. (New) The bi-directional shift controller circuit as recited in claim 16, wherein said shift register stages are physically adjacent to said bi-directional controller.

31. (New) The bi-directional shift controller circuit as recited in claim 16, wherein said shift register stages are logically adjacent to said bi-directional controller.